REMARKS/ARGUMENTS

This Amendment is submitted in response to the second, but non-final, Official Action dated September 2, 2005. Reconsideration and allowance of claims 1-4 in light of the foregoing amendments and these accompanying Remarks are respectfully requested.

The Office Action rejects Claims 1 and 3 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 4,801,561 to Sankhagowit. As I am sure the Examiner appreciates, before it is appropriate to reject a claim as anticipated under 35 U.S.C. §102(b) the reference relied upon must disclose each and every element and limitation of the claim sought to be anticipated. Element (a) of claims 1 and 3 requires a TAB tape frame having a predetermined conductive test pad footprint formed about a perimeter of the TAB tape frame and a bond pad footprint generally centrally disposed relative to the test pad footprint and that there also be conductive leads that connect the bond pads individually to the test pads and to ball grid array pads that are generally centrally disposed relative to the bond pad footprint. While the Sankhagowit '561 patent shows TAB tape frames with the claimed test pad and bond pad footprints, it fails to teach or suggest ball grid array pads connected by conductive leads to the bond pads and the test pads. As such, the cited '561 patent does not anticipate claims 1 and 3 as contended in the Office Action.

Next, independent claims 1 and 3 are also rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,343,366 to Cipolla et al. For the same reason that claims 1 and 3 are not anticipated by the Sankhagowit '561 reference, they are also not anticipated by Cipolla et al. Cipolla fails to teach an array of ball grid pads that are connected by conductive leads to bond pads and test pads as set forth in element (a) of applicant's claims 1 and 3. Thus, the rejection of independent claims 1 and 3 based on the Cipolla et al. patent should be withdrawn.

Claims 1-4 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,249,052 to Lin. This rejection is also respectfully traversed.

As those skilled in the art appreciate, Tape Automatic Bonding (TAB) is a process wherein silicon chips are joined to patterned metal traces (leads) on polymer tape to form

inner lead bonds and, subsequently, the leads are attached to the next level of the assembly, typically a substrate or board to form outer lead bonds. The Lin et al. Patent describes a different type of lead frame for mounting a silicon chip. As shown in Figure 1A of the Lin '052 patent, an integrated circuit chip 101 is attached by an adhesive layer 102 to the undersurface of a laminated PC board 103 that has a window 104 through which bonding wires 104' connect the bonding pad on the IC chip 101' to a bonding pad on the PC board 103' via connector 106 extends through the thickness dimension of the laminated PC board 103 to make contact with an array of solder balls 130.

It is believed inappropriate to refer to the PC board 103 of the Lin '052 patent as a TAB tape frame called for by element (a) of independent claims 1 and 3.

Step (d) of independent claims 1 and 3 now calls for over-molding the **entire** semiconductor die and the bond pad footprint with a plastic to form the integrated circuit module. In the Lin '052 arrangement, the plastic 108 encapsulates only the portion of the integrated circuit chip that is exposed through the window 104 in the printed circuit board 103. Claims 1-4, as amended, specify that the entire semiconductor die be over-molded along with the bond pad footprint. Since the Lin '052 patent does not meet this limitation, it does not anticipate claims 1-4 within the meaning of 35 U.S.C. §102(b).

Further, and as set forth at page 2 of applicant's specification, in the case of the present invention, input/output points of the semiconductor chip are connected by conductive leads routed on the TAB tape first to ball grid array pads internal to the outline of the chip and secondly to test pads located external to the semiconductor package outline. As such, the test pads can be used during test and burn-in, making it unnecessary to have special BGA sockets to hold the device during test and burn-in. As is indicated at column 7, line 66 through column 8, line 20 of the Lin patent, testing of the Lin device requires a "standard testing socket" for performing a burn-in test and a board level test. This is just the method that the present invention has been designed to overcome.

For the reasons advanced, then, it is submitted that none of the three cited references can be said to fairly anticipate any of claims 1-4, and unless further searching uncovers more relevant prior art, a Notice of Allowance should be issued.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that the foregoing Amendment is filed in response to the Official Action of September 2, 2005, in application Serial No. 10/782,505, filed on February 18, 2004, of James E. Blood, entitled "Method for Preparing Integrated Circuit Modules for Attachment to printed Circuit Substrates" is being deposited with the U.S. Postal Service as First Class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, postage prepaid, on December 1, 2005.

Date of Signature: December 1, 2005.

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